REMARKS/ARGUMENTS

Applicants have received the Office action dated September 29, 2004, in which the Examiner: (1) rejected claims 1-13 under the judicially created doctrine of obviousness-type double patenting; (2) rejected claims 8-13 under 35 U.S.C. § 102(e) as allegedly being anticipated by Adusumilli (U.S. Pat. No. 6,704,817); and (3) despite the double patenting rejection, allowed claims 1-7. With this Response, Applicants submit a terminal disclaimer and traverse the rejection of claims 8-13 over Adusumilli. Based on the arguments contained herein, Applicants believe all pending claims to be in condition for allowance.

I. DOUBLE PATENTING

Applicants do not concede the merits of the Examiner's double patenting rejection, but to expedite prosecution, opt not to address the merits of the rejection. Instead, Applicants submit herewith a Terminal Disclaimer.

II. REJECTIONS OF CLAIMS 8-13 OVER ADUSUMILLI

Adusumilli is directed to solving the problem of delayed read transactions being "discarded" upon the occurrence of write transaction. While discarding the delayed read transaction may be required to avoid a data coherency problem, discarding read transactions can reduce system performance. For example, "glitches" may appear on a monitor as a result of delayed reads of graphics data being discarded in favor of write transactions. See Cols. 1 and 2.

The Examiner identified specific passages in Adusumilli as allegedly teaching the limitations of claim 8. Table I below compares the limitations of claim 8 on the left to the passages from Adusumilli cited by the Examiner on the right.

TABLE I.

CLAIM 8	Passages from Adusumilli cited by Examiner as allegedly reading on the claim associated limitations
Tracking the number of pending writes in a write queue;	"In this situation an inhibited write transaction is performed during which read/write optimizing circuit 100 tracks an inhibited write transaction target address of the write request until an appropriate condition for final

TABLE I.

CLAIM 8	Passages from Adusumilli cited by Examiner as allegedly reading on the claim associated limitations
	processing occurs." Col. 5, lines 29-33.
Tracking the number of pending reads in a read queue;	"In this situation an inhibited write transaction is performed during which read/write optimizing circuit 100 tracks an inhibited write transaction target address of the write request until an appropriate condition for final processing occurs." Col. 5, lines 29-33.
Tracking the number of consecutively issued reads when the number of pending writes reaches a pending write threshold;	"A special sequence of address transfers occurs in instances in which a prior PCI transaction was a read transaction resulting in a pending read situation and a current PCI transaction is a write transaction including postable write information that arrives before the pending read transaction is completed or terminated." Col. 5, lines 23-29. "PCI target control 110 tracks incremental changes in the write address.." Col. 5, line 67 to col. 6, line 1.
Tracking the number of consecutively issued writes when the number of pending reads reaches a pending read threshold;	"A special sequence of address transfers occurs in instances in which a prior PCI transaction was a read transaction resulting in a pending read situation and a current PCI transaction is a write transaction including postable write information that arrives before the pending read transaction is completed or terminated." Col. 5, lines 23-29. "PCI target control 110 tracks incremental changes in the write address..." Col. 5, line 67 to col. 6, line 1.
Transitioning from issuance of reads to	"PCI target control component 110

TABLE I.

CLAIM 8	Passages from Adusumilli cited by Examiner as allegedly reading on the claim associated limitations
issuance of writes when the number of pending writes reaches said pending write threshold and the number of consecutively issued reads reaches a consecutively issued read threshold; and	directs communication operations in accordance with PCI protocols and controls the loading of information in read FIFO buffer 130, write FIFO buffer 120 and second address register PADR 175 via MUX 185." Col. 4, lines 35-40.
Transitioning from issuance of writes to issuance of reads when the number of pending reads reaches said pending read threshold and the number of consecutively issued writes reaches a consecutively issued write threshold.	"PCI target control component 110 directs communication operations in accordance with PCI protocols and controls the loading of information in read FIFO buffer 130, write FIFO buffer 120 and second address register PADR 175 via MUX 185." Col. 4, lines 35-40.

Applicants disagree with the Examiner's assessment that all limitations of claim 8 are found in Adusumilli. In fact, Applicants believe none of the limitations are found in Adusumilli. The first two claim limitations relate to "tracking the number" of pending writes and reads. As noted by the Examiner, Adusumilli teaches that the "optimizing circuit 100 tracks an inhibited write transaction target address of the write request." Tracking the number of pending writes and the number of pending reads as in claim 8 is patentably different from tracking a write transaction address as in Adusumilli.

The next two limitations in claim 8 relate to "tracking the number of consecutively issued reads" and "the number of consecutively issued writes." The passages cited by the Examiner as allegedly teaching these limitations do not at all teach or even suggest these limitations. The cited passage does not teach "tracking a number of" anything, much less the number of consecutively issued reads/writes.

The last two limitations in claim 8 relate to transitioning between issuance of reads and writes based on the numbers tracked in the preceding limitations. The passage cited by the Examiner clearly does not read on these limitations.

For any or all of these reasons, claim 8 and all claims dependent from claim 8 are allowable over Adusumilli. None of the other art of record appears to satisfy the deficiencies of Adusumilli. Further, in allowing claims 1-7 the Examiner concluded that there was no "motivation to combine any of the said prior arts." That being the case, the Examiner has gone on record to preclude combining the art of record to render obvious claim 8 and its dependent claims.

System claim 11 requires "control logic" that operates "to reduce the number of transitions between read transactions and write transactions." For this limitation, the Examiner turned to Figure 1 (control 110) and col. 4, lines 35-40. The cited passage from Adusumilli is as follows: "PCI target control component 110 directs communication operations in accordance with PCI protocols and controls the loading of information in read FIFO buffer 130, write FIFO buffer 120 and second address register PADR 175 via MUX 185." This passage says nothing about reducing the number of transitions between read transactions and write transactions. At least this reason, claim 11 and dependent claims 12-13 are allowable over Adusumilli. None of the other art of record satisfy the deficiency of Adusumilli and the Examiner, as noted above, has precluded combining the art of record to render obvious claim 11.

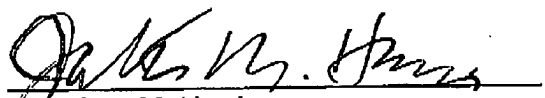
III. CONCLUSION

In the course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the cited art which have yet to be raised, but which may be raised in the future.

Appl. No. 10/780,395
Amdt. dated December 29, 2004
Reply to Office action of September 29, 2004

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

Respectfully submitted,



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